Remarks

In the specification, the paragraph at page 6, line 15, has been amended to correct minor typographical errors (re-numbering of the gate oxide layer from *14* to *16*). Support for the amendment is in the specification at page 6, lines 7-14 (emphasis added), and FIG. 2 (below).

> The wafer fragment 10 is shown as comprising a semiconductor substrate 12, an exemplary substrate being a bulk substrate material of semiconductive or semiconductor material, for example, monocrystalline silicon. The substrate 12 is provided with isolation regions 14 formed therein, for example, shallow trench isolation regions. A gate oxide (dielectric) layer 16 overlies the substrate 12. The gate oxide layer 16 can comprise, for example, silicon dioxide (SiO_2), tantalum pentoxide (Ta_2O_5), hafnium dioxide (HfO_2), and aluminum trioxide (Al_2O_3), among others. *The gate oxide layer 16* can be formed by conventional methods, and is typically an oxide layer grown directly on the base silicon substrate material 12, but can also be a deposited layer.

Reconsideration of pending Claims 1-57 and 73-121 is respectfully requested.

Claims 1, 5-9, 16-20, 23, 25-28, 36-39, 41-47, 49, 51-53, 73, 75-76, 80-83, 85-92, and 97 have been amended. Support for the amendments is discussed below. No new matter has been added with the amendments to the claims, which are intended to merely clarify language used in the claims and/or the subject matter claimed. The scope of the claims is intended to be the same as before the amendment.

Rejection of Claims under 35 U.S.C. § 112(1)

The Examiner rejected Claims 1-14, 16-21, 97-100, 103-106, and 112 under Section 112(1) as non-enabled.

The Examiner maintains that the following phrases are not described/supported by the original specification:

a) "the silicon layer and silicon nitride layer having a combined thickness of about 10-30 angstroms" (Claims 1, 5, 7-9, 16-18);

b) "the combined thickness of the silicon layer and silicon nitride layer is about 10 to about 20 angstroms" (Claim 6), and

c) "the nitridized silicon layer having a thickness of about 10-30 angstroms" (Claims 19-20).

The claims have been amended to more clearly indicate that *the nitride barrier layer* has a thickness of about 10 to less than about 30 angstroms, or about 10-20 angstroms.

Support for the amendments to the claims is in the specification at pages 3-4, bridging sentence ("...the nitride barrier layer comprises thermally annealed nitridized silicon having a thickness of about 10 to about 20 angstroms..."), at page 4, line 5 ("...a diffusion barrier layer of about 10 to about 20 angstroms..."), at page 4, lines 14-15 ("...the diffusion barrier layer having a thickness of about 10 to about 20 angstroms..."), and the claims as originally filed (e.g., Claim 59: A nitride barrier layer, comprising: a nitridized silicon layer having a thickness of less than about 30 angstroms...).

The Examiner also maintains that the terms "continuous" and "uniform" with regard to the silicon layer (Claims 1, 5, 7, 8, 9, 16-20) are not supported by the original specification.

The Examiner's position is *incorrect.* The term "continuous" or "uniform" layer of silicon **18** is clearly illustrated and fully supported in the specification and in Applicant's **FIG. 2**, as shown below.

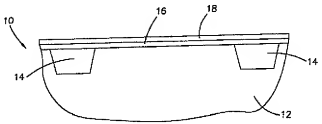

FIG. 2

As described in the specification at page 6, lines 15-26 (*as amended;* emphasis added):

> According to the invention, the gate oxide layer 16 is irradiated with a silicon containing species under low partial pressure, high vacuum conditions to deposit (nucleate) *a thin layer 18 of silicon onto the surface of the gate oxide layer 16, as shown in FIG. 2.* The silicon layer can comprise polysilicon or amorphous silicon. The processing conditions results in a silicon layer 18 that is thinner than can be achieved under standard silicon growth conditions...Preferably, the silicon layer 18 is less than about 30 angstroms, preferably about 10 to about 20 angstroms thick....The silicon material can be deposited as a layer utilizing any known deposition process including plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), and rapid thermal chemical vapor deposition (RTCVD).

FIG. 2 clearly illustrates a silicon layer **18** that is *continuous* and/or *uniform* over the surface of the gate oxide layer **16** – *versus* a *non*-continuous material layer made of separate or disconnected portions.

Reading Applicant's disclosure, one of ordinary skill in the art would readily understand the meaning of a "continuous" or "uniform" silicon layer (18) versus a non-continuous or non-uniform material layer.

This is further supported, for example, in the background discussion in USP 6,297,095 (Muralidhar), cited by the Examiner. In the background discussion, Muralidhar discusses "uniform" layers of polysilicon and distinguishes them from a layer composed of *unconnected and isolated nanoclusters* of polysilicon. See at col. 1, line 52 to col. 2, line 24 (emphasis added):

> *In many prior art device structures, the floating gate is formed from a uniform layer of material such as polysilicon*. In such prior art device structures, a thin tunnel dielectric layer beneath the floating gate presents the problem of charge leakage from the floating gate to the underlying channel through defects in the thin tunnel dielectric layer. Such charge leakage can lead to degradation of the memory state stored within the device and is therefore undesirable. In order to avoid such charge leakage, the thickness of tunnel dielectric is often increased. However, thicker tunnel dielectric requires higher (programming and erasing) voltages for storing and removing charge from the floating gate as the charge carriers must pass through the thicker tunnel dielectric. In many cases, higher programming voltages require the implementation of charge pumps on integrated circuits in order to increase the supply voltage to meet programming voltage requirements. Such charge pumps consume a significant amount of die area for the integrated circuit and therefore reduce the memory array area efficiency and increase overall costs.
>
> In order to reduce the required thickness of the tunnel dielectric and improve the area efficiency of the memory structures by reducing the need for charge pumps, *the uniform layer of material used for the floating gate may be* ***replaced*** *with a plurality of nanoclusters, which operate as* ***isolated*** *charge storage elements*. Such nanoclusters are also often referred to as nanocrystals, as they may be formed of silicon crystals. In combination, the *plurality of nanoclusters* provide adequate charge storage capacity *while remaining physically isolated from each other* such that any leakage occurring with respect to a single nanoclusters via a local underlying defect does not cause charge to be drained from other nanoclusters (by controlling average spacing between nanoclusters, it can be ensured that there is no lateral charge flow between nanoclusters in the floating gate). As such, thinner tunnel dielectrics can be used in these device structures. The effects of leakage occurring in such thin tunnel dielectric devices does not cause the loss of state information *that occurs in devices that include a uniform-layer floating gate*.

Muralidhar distinguishes a "uniform" polysilicon layer from a layer formed of discontinuous and isolated nanoclusters of polysilicon.

Applicant has provided a sufficiently enabling disclosure, both in the figures and descriptive discussion, to teach those of ordinary skill in the art how to make and use the invention as broadly as it is claimed, and to meet the requirements of 35 U.S.C. 112, first

paragraph. Applicant submits that the specification is sufficiently enabling for one of ordinary skill in the art to make and use the invention disclosed and claimed without undue experimentation.

One skilled in the art reading Applicant's disclosure and based on the understanding within the art, would readily ascertain Applicant's method as claimed.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejection of Claims under 35 U.S.C. § 102(b) (Muralidhar)

The Examiner maintains the rejection of Claims 1-14, 16-19, 97-100, 103-104, 106, and 112 under Section 102(e) as anticipated by USP 6,297,095 (Muralidhar). The Examiner also maintains the rejection of Claims 20-21 and 105 under Section 103(a) as obvious over Muralidhar. These rejections are respectfully traversed.

In the Office Action at page 13, the Examiner stated as follows:

> Applicant stated that the support for the new added limitations in the claims can be found at page 4, lines 14-15, and page 6, lines 21-22 and the drawing (i.e., Fig. 2, silicon layer 18). The Examiner respectfully disagrees because none of the cited places show 1) forming a **continuous** or **uniform** layer of silicon, 2) the **silicon layer** and **silicon nitride layer** having a combined thickness of about **10-30 angstroms (or 10-20 angstroms)** and 3) the nitridized silicon layer having a thickness of about 10-30 angstroms.

Muralidhar describes the fabrication of a memory device composed of a plurality of silicon *nanoclusters* **104** that form a *floating gate* of a memory device.

First of all, Muralidhar does not teach or suggest forming a *continuous* or *uniform* silicon layer over an oxide layer – as described and claimed by Applicant.

Rather, Muralidhar teaches depositing *physically isolated* nanoclusters of silicon **104** on a dielectric layer **102** – as shown below in **FIG. 22** below.

FIG.22

Importantly, Muralidhar particularly distinguishes a *uniform layer* of polysilicon from *unconnected and isolated nanoclusters* of polysilicon. See the above excerpt from Muralidhar at col. 1, line 52 to col. 2, line 24.

In addition, Muralidhar does not teach of suggest forming a *nitride barrier layer* having a thickness of about 10 to less than about 30 angstroms, or about 10-20 angstroms, as recited in the claims.

Rather, Muralidhar teaches forming a *thin* nitride layer **106/107** -- of up to only *5 angstroms* over the silicon nanoclusters **104**. This is described at col. 16 at lines 45-48, and col. 17 at lines 13-23 (emphasis added), and illustrated in **FIGS. 23 and 25** below, and:

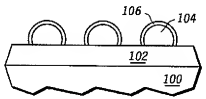

FIG.23

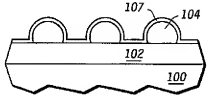

FIG.25

...

Preferably, the formation of the encapsulation layer **106** can be controlled such that the *thickness of the encapsulation layer **106** is on the order of 5 angstroms*, or no greater than 10% of the diameter of the nanoclusters **104**. ...

...In other embodiments, a protecting nitride layer may be deposited rather than grown on individual nanoclusters. **FIG. 25** illustrates the nanocluster structures as shown in FIG. 22 following a step where a thin nitride layer **107** is deposited. ...*A desirable thickness for the thin nitride layer **107** may be on the order of 5 angstroms*. ...

Muralidhar does not teach or suggest Applicant's methods of forming a nitride barrier layer by (a) depositing a *continuous* (or uniform) layer of silicon on a dielectric layer, and (b) exposing the silicon layer to a nitrogen gas to form a silicon nitride barrier layer having a *thickness* of about *10 angstroms up to less than about 30 angstroms, or about 10-20 angstroms.*

Muralidhar does not teach or suggest Applicant's methods as claimed. Accordingly, withdrawal of the rejections based on Muralidhar is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required.

However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

It is respectfully submitted that the claims are in condition for allowance and notification to that effect is earnestly solicited.

Respectfully submitted,

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Dated: July 31, 2006

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